**Lab 03**

**INTRODUCTION TO XILINX ISE, Spartan 6 BOARD AND IMPLEMENTATION OF RIPPLE CARRY ADDER AND FULL SUBTRACTOR**



**Spring 2025**

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Class Section: **A**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”



Student Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

**Engr. Faheem Jan**

Month Day, Year (16 02, 2025)

Department of Computer Systems Engineering

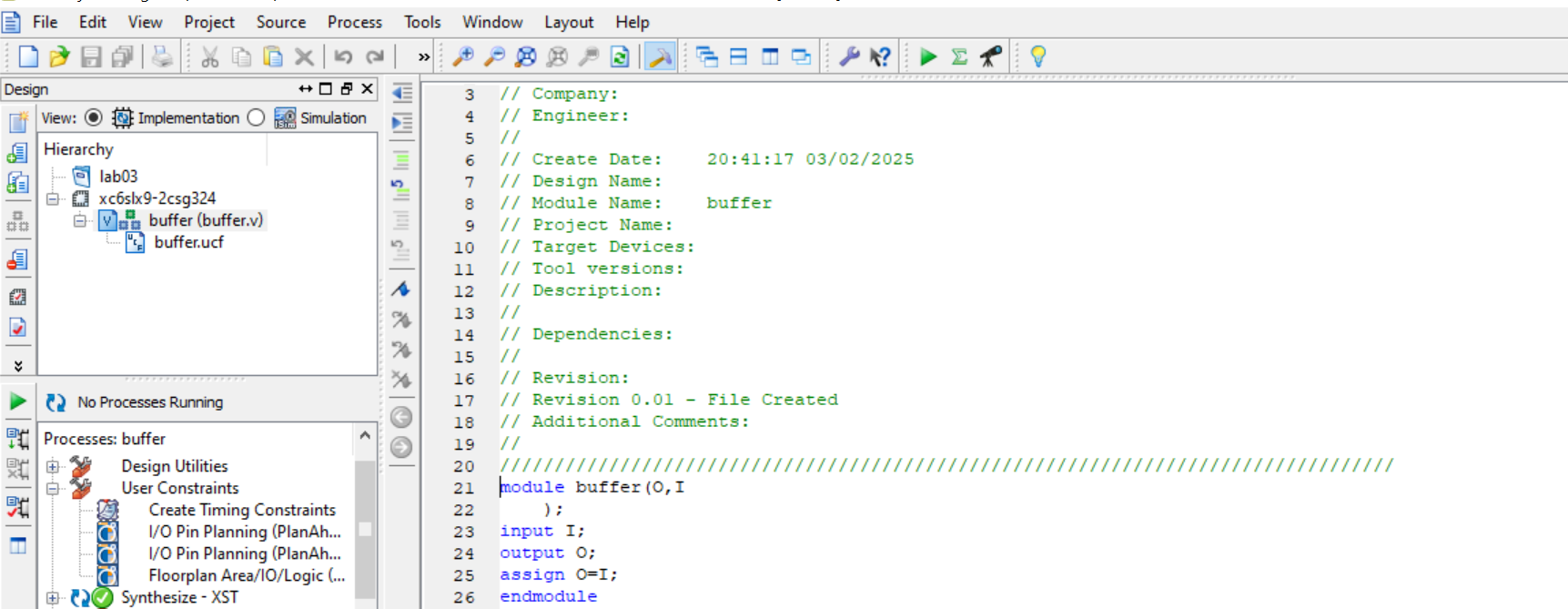
University of Engineering and Technology, Peshawar

**Objectives:**

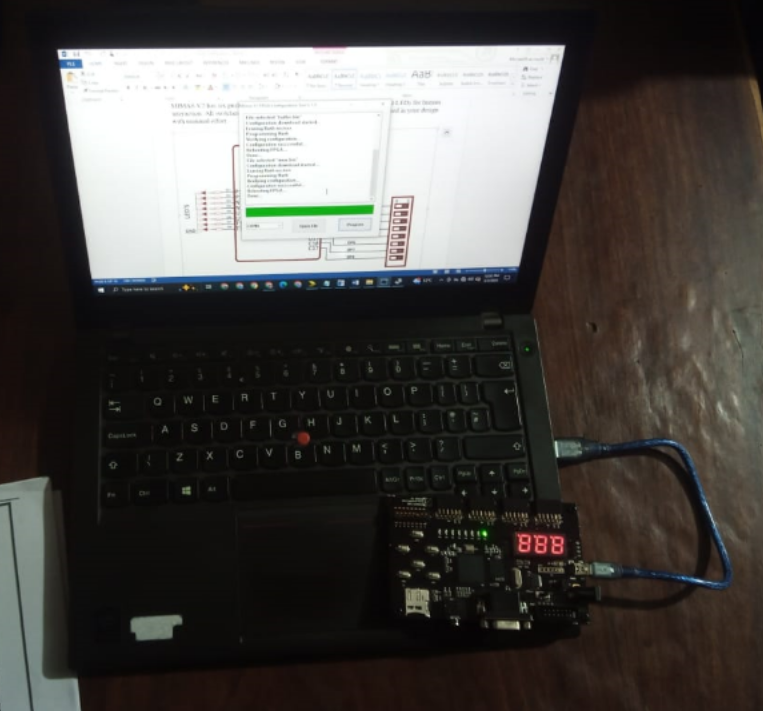
* Introduction to FPGA
* Introuction Xilinx ISE

LAB TASKS:

1-Implement buffer ON the Kit and attach the snapshot.

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**Output on Xilinx:**

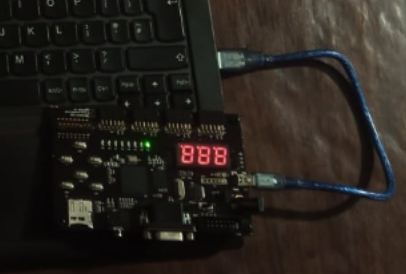
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2-Implement AND/OR/XOR gate on the Kit and attach the snapshot.

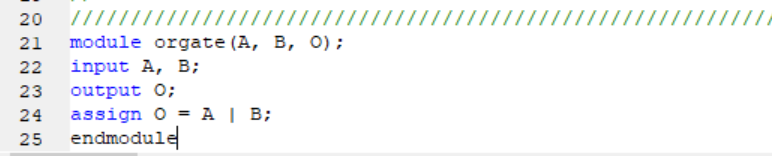
**And Gate:**



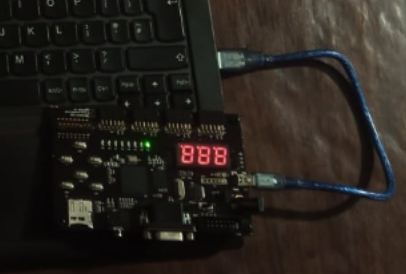
**Output:**

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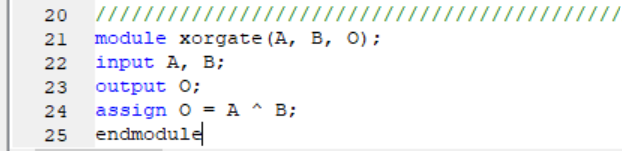
**OR Gate:**

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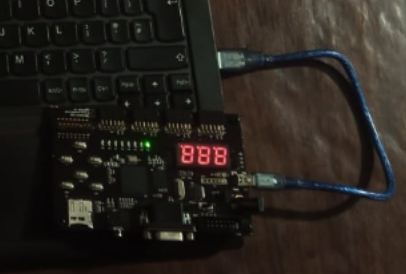
**Output:**

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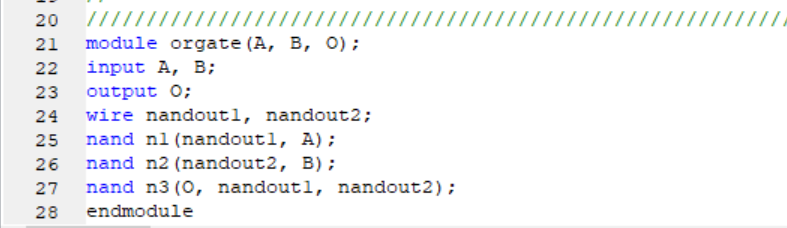
**XOR Gate:**

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**Output:**

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**3-Impement OR gate using NAND gate**

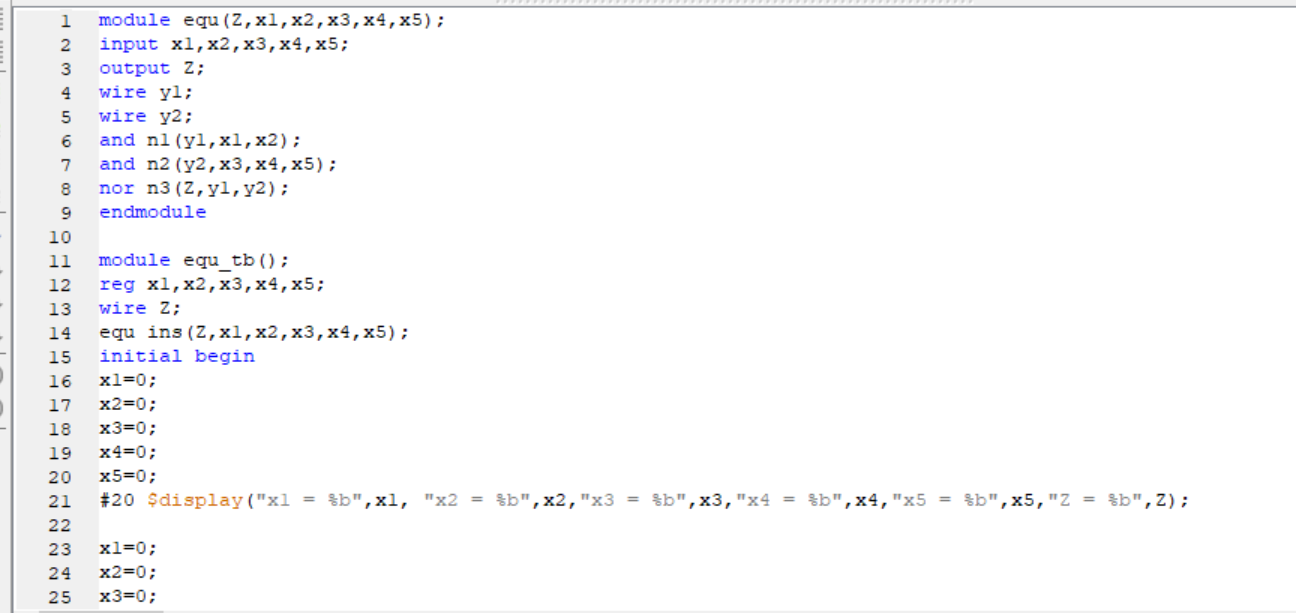


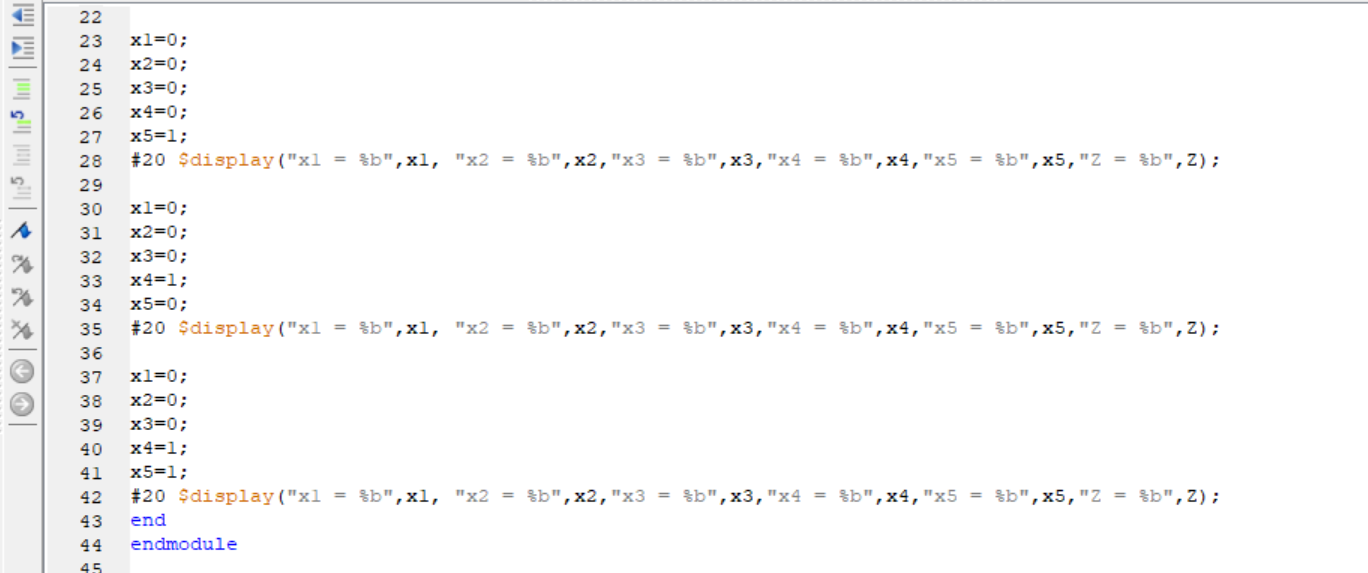
**Output Xilinx:**



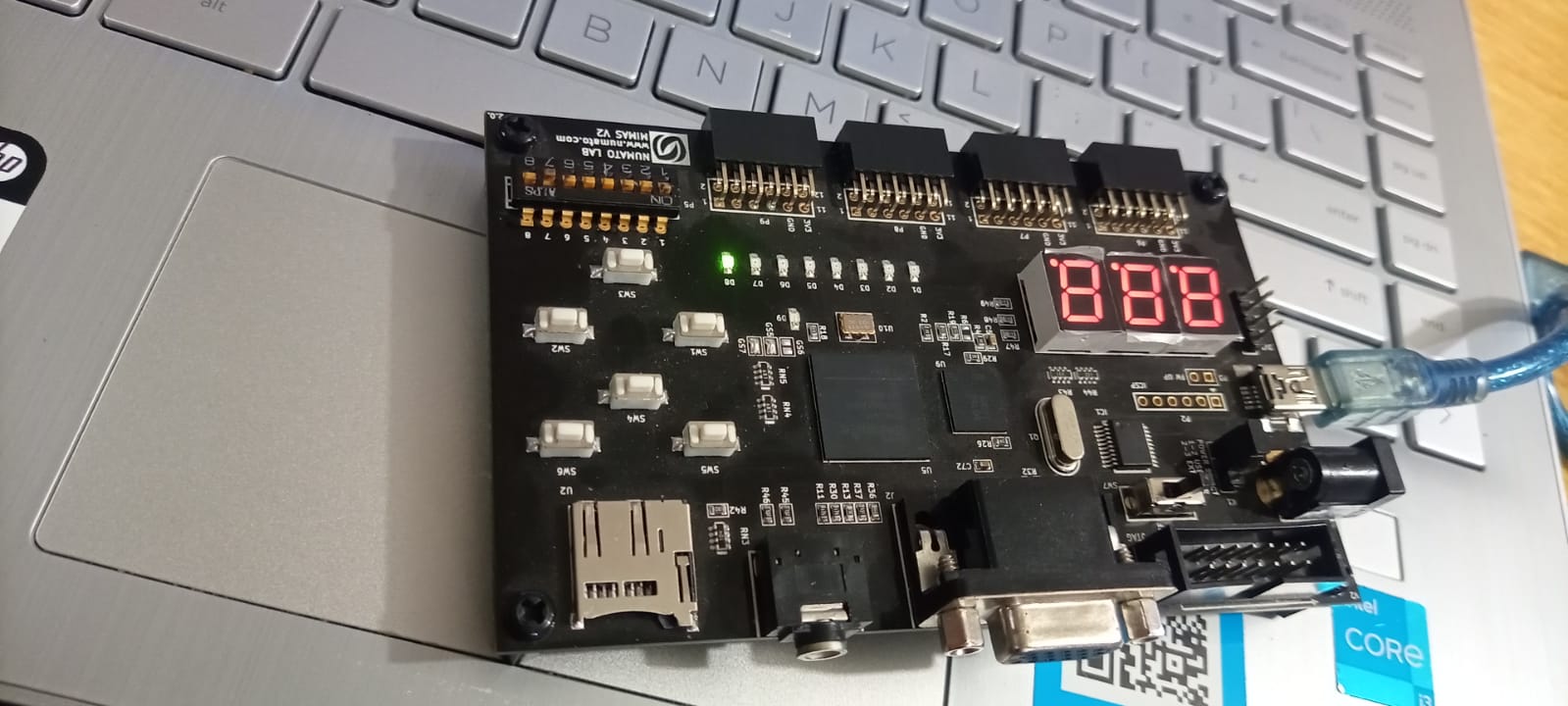
**4- Implement Lab1 and Lab1 ON the Kit and attach snapshot.**

**Equation:**

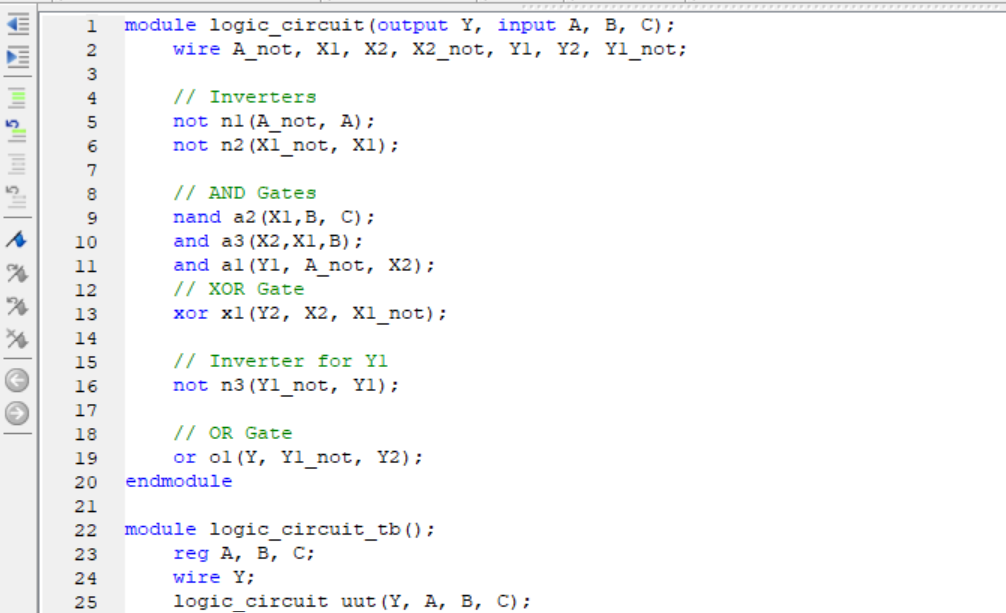
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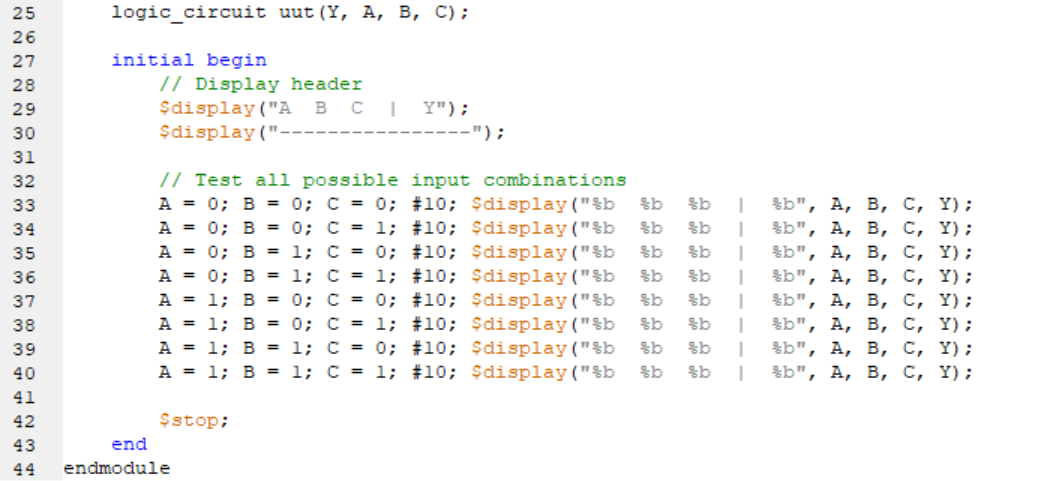
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**Xilinx output:**



**Logic Circuit:**

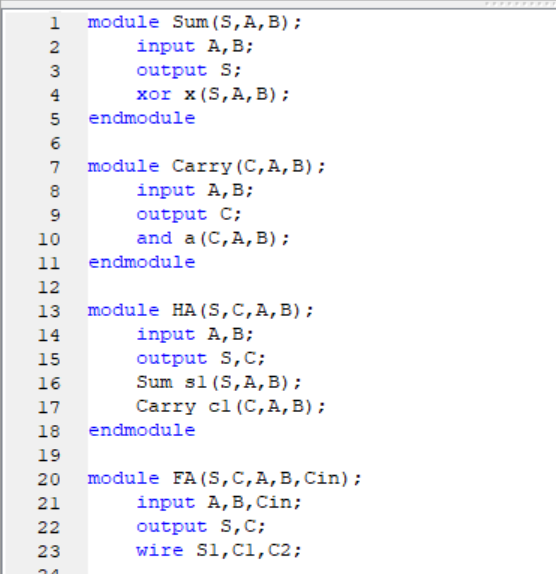
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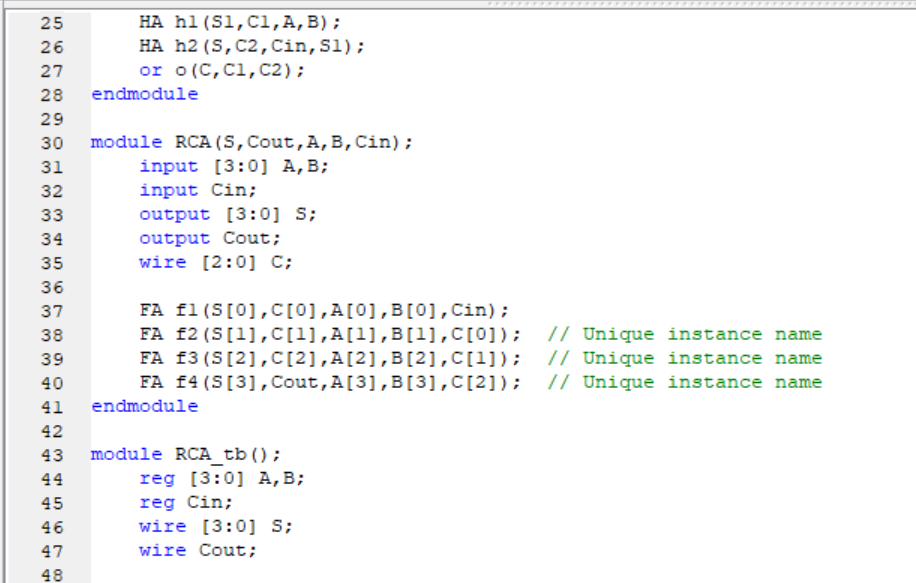
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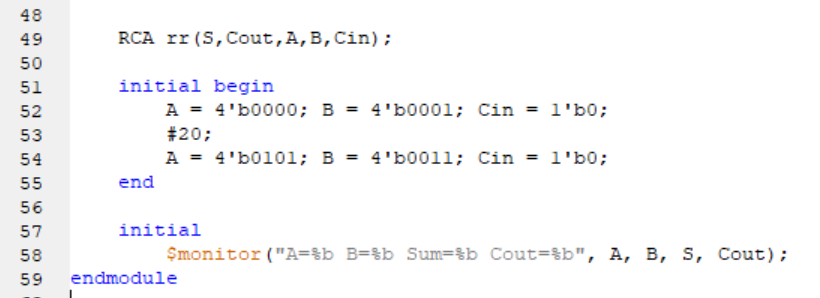
**Xilinx Output:**

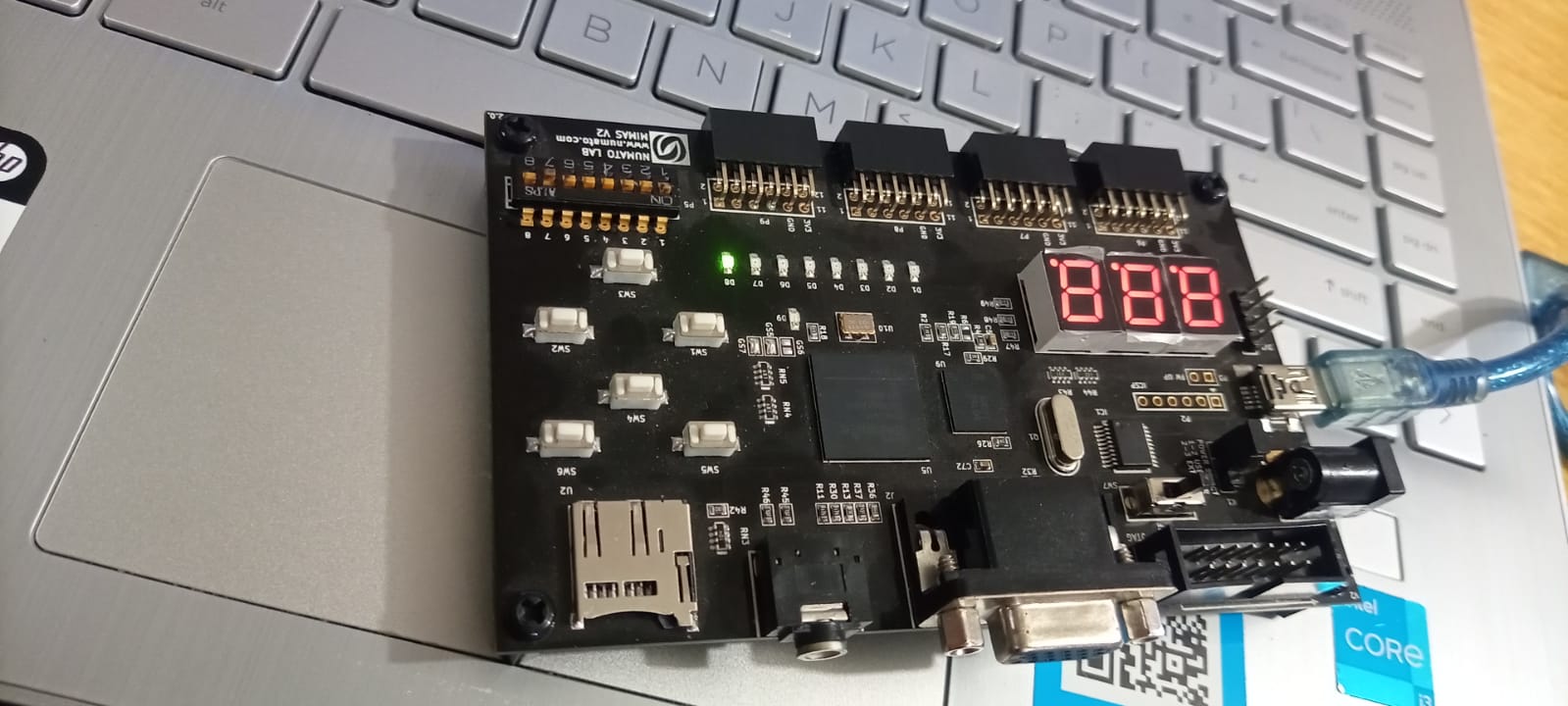
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**Ripple Carry Adder:**

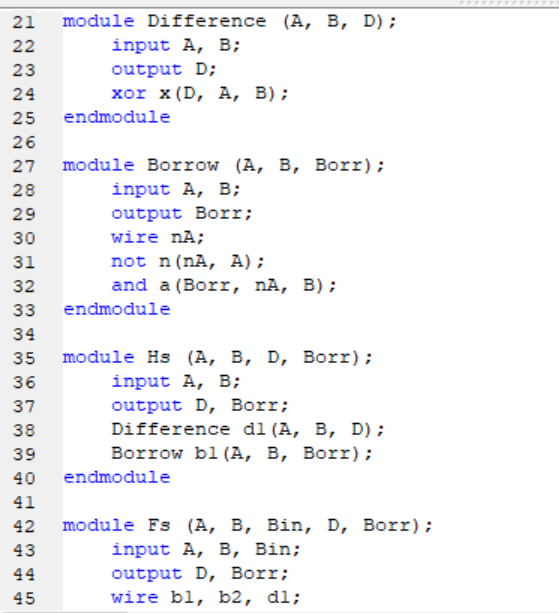
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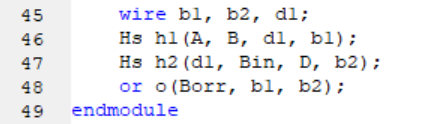
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**5- Implement Full Subtractor on the board and verify the truth table**





**Output Xilinx:**

